UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/688,203	10/16/2000	Kenichiro Nakagawa	NEC00P264-ks	8790

21254 7590 04/25/2003

MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER
BREWSTER, WILLIAM M

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/688,203	NAKAGAWA, KENICHIRO	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Petition

Applicant's request for reconsideration of the finality of the rejection, in Paper No. 9, received 3 March 2003, of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-4, and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Yaegashi et al., U.S. Patent No. 6,265,739.

Yaegashi anticipates a method of manufacturing a semiconductor memory device capable of electrically writing and erasing data, said semiconductor memory

device having a plurality of cell transistors for storing data, in fig. 1 and 2A, forming gate insulating films 105 of transistors of a peripheral circuit comprising a logic operation circuit VCC-Tr, simultaneously with the gate insulating films of said select transistors SELECT TRANSISTORS, each of said cell transistors MEMORY CELL having a floating gate electrode 106 and a control gate electrode 107, both made of polysilicon, col. 8, lines 5-29, and a plurality of select transistors for controlling and selecting said cell transistors, col. 7, line 57 - col. 8, line 54, said method comprising: in fig. 2A, before forming the control gate electrodes of said cell transistors, exposing a surface of a substrate directly above channel regions of said select transistors fabricated in the same process as the cell transistors (examiner, duty bound to interpret claim limitations broadly, interprets this step as being the cleaning step performed in all wafer fabrication before any processing step occurs); forming gate insulating films 105 of transistors of a peripheral circuit comprising a logic operation circuit, simultaneously with the gate insulating films of said select transistors, and in fig. 2A forming gate electrodes 106 of the transistors of said peripheral circuit simultaneously with the gate electrodes 106 of said select transistors before forming the control gate electrodes of said cell transistors, in figs. 10A, B, C, simultaneously forming a first diffused layer serving as source and drain regions n- of said cell transistors and a second diffused layer serving as source and drain regions of said select transistors exposing a surface of a substrate directly above channel regions of said select transistors fabricated in the same process as the cell transistors, col. 11, lines 17 - 27; in figs. 4A-B, forming gate electrodes of the transistors of said peripheral circuit VCC-Tr simultaneously with the gate electrodes of

said select transistors, SELECT TRANSISTORS, in fig. 2C, forming gate insulating films of said select transistors on the exposed surface of the substrate; forming the control gate electrodes 107 of said cell transistors and forming gate electrodes of said gate insulating films, col. 8, line 62 - col. 9, line 45.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yaegashi as applied to claim 1-4 above, and further in view of Chen et al., U.S. Patent No. 5,824,584.

Yaegashi does not teach forming the gate insulating thicknesses of the select and peripheral circuits equivalently, but Chen does. Chen teaches in figs. 1-6, the method of manufacturing a semiconductor memory device wherein the gate insulating films 12 of said select transistors 16 have a film thickness which is the same as the film thickness of the gate insulating film of a transistor which requires a high withstand voltage, among the transistors of said peripheral circuit, between 30-300 Å, col. 3, lines 16 - 37. Chen gives motivation in col. 2, line 54 - col. 3, line 8. It would have been

obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Chen's process with Yaegashi 's invention would have been beneficial because allows the implementation of logic and memory cells on a common substrate without increasing the number of processing steps.

Response to Arguments

Applicant's arguments with respect to claims 1-6 have been considered but are not persuasive. Applicant argues on pages 2 and 3 of Paper No. 10, that Yaegashi does not anticipate the limitation in claim 1, lines 6-8, "before forming the control gate electrodes of said electrodes of said cell transistors, exposing a surface of a substrate directly above channel regions of said select transistors fabricated in the same process as the cell transistors".

Examiner disagrees. While applicants may believe this reflects steps delineated by application figures 16-19, it may be reasonably interpreted to mean the step as being the cleaning step performed in all wafer fabrication before any processing step occurs which takes place before the control gate electrodes are formed to expose the substrate in the same process as the cell transistors.

Examiner must give claims their broadest reasonable interpretation, MPEP §2111, "During patent examination, the pending claims must be 'given the broadest reasonable interpretation consistent with the specification.' Applicant always has the opportunity to amend the claims during prosecution and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more

broadly than is justified, *In re Pratter*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969), *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997)." Also see *In re Zletz*, 13 USPQ 2d. 1320 (Fed. Cir. 1989).

Examiner will consider the proffered inventive step when the claims more narrowly define it to only mean the steps delineated by application figures 16-19.

For the above reasons, the §102(e) and §103(a) rejections of above are considered proper.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 703-305-5906. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-3432 for regular communications and 703-305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800

WB

April 2, 2003